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WELLS ST. JOHN ROBERTS GREGORY & MATKIN P.S.  
601 W. FIRST AVENUE  
SUITE 1300  
SPOKANE, WA 99201-3828

EXAMINER

VU, QUANG D

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/652,550

Applicant(s)

JONO ET AL.

Examiner

Quang D Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_ 6) ☐ Other: \_\_\_\_

## **DETAILED ACTION**

### ***Claim Objections***

Claim 10 is objected to because of the following informalities: In lines 1-2, the phrase "...forming a first isolation trench portion comprises forming a first isolation trench portion..." should be changed to "...forming said first isolation trench portion comprises forming said first isolation trench portion...". Appropriate correction is required.

Claim 12 is objected to because of the following informalities: In lines 1-2, the phrase "...forming a first isolation trench portion comprises forming a first isolation trench portion..." should be changed to "...forming said first isolation trench portion comprises forming said first isolation trench portion...". Appropriate correction is required.

Claim 14 is objected to because of the following informalities: In line 2, the phrase "...forming a first isolation trench portion having..." should be change to "...forming said first isolation trench portion having...". Appropriate correction is required.

Claim 15 is objected to because of the following informalities: In lines 1-2, the phrase "...forming a first isolation trench portion comprises forming a first isolation trench portion including..." should be change to "...forming said first isolation trench portion comprises forming said first isolation trench portion including...". Appropriate correction is required.

Claim 17 is objected to because of the following informalities: In lines 1-2, the phrase "...forming a first isolation trench portion comprises forming a first isolation trench portion having..." should be changed to "...forming said first isolation trench portion comprises forming said first isolation trench portion having...". Appropriate correction is required.

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Claim 23 is objected to because of the following informalities: In lines 1-2, the phrase "...forming a first isolation trench portion comprises etching..." should be changed to "...forming said first isolation trench portion comprises etching...". Appropriate correction is required.

Claim 27 is objected to because of the following informalities: In lines 1-2, the phrase "...forming a first isolation trench portion comprises forming a first isolation trench portion having..." should be changed to "...forming said first isolation trench portion comprises forming said first isolation trench portion having...". Appropriate correction is required.

Claim 32 is objected to because of the following informalities: In lines 1-2, the phrase "...forming a gate comprises forming a gate comprising polysilicon" should be changed to "...forming said gate comprises forming said gate comprising polysilicon". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4, 5-7, 9, 20, 24, 25-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the phrase "...forming an isolation trench in a semiconductor comprises forming an isolation trench in silicon". It is unclear whether the isolation trench of claim 1 is formed in a semiconductor comprises silicon.

Claim 5 recites the phrase “forming a masking layer having an opening disposed therein atop the silicon nitride layer...” in lines 4-5. The specification discloses a photoresist layer having an opening disposed on the top of the silicon nitride layer. The specification never discloses a masking layer having an opening disposed on the top of the silicon nitride layer.

Claim 9 recites the phrase “forming a masking layer having an opening disposed therein atop the silicon nitride layer...” in lines 4-5. The specification discloses a photoresist layer having an opening disposed on the top of the silicon nitride layer. The specification never discloses a masking layer having an opening disposed on the top of the silicon nitride layer.

Claim 20 recites the phrase “...continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls...” in lines 4-6. It is unclear whether the plasma etching step of the silicon nitride layer and the polymer deposition step are performed simultaneously or they are sequenced one after another.

Claim 24 recites the phrase “...forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls” in lines 3-4. The specification discloses a photoresist layer having an opening disposed on the top of the silicon nitride layer. The specification never discloses a masking layer having an opening disposed on the top of the silicon nitride layer.

Claim 25 recites the phrase “...plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls; continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls...” in lines 3-7. It is unclear whether the same conditions are being used for the plasma etching step and the polymer deposition step. In addition, it is unclear whether the

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plasma etching step of the silicon nitride layer and the polymer deposition step are performed simultaneously or they are sequenced one after another.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-4, 10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,274,457 to Sakai et al.

Regarding claim 1, Sakai et al. (figures 1, 2a-f, 3) teach a method of forming an isolation trench in a semiconductor comprising:

forming a first isolation trench portion (a trench portion that has an angle of A1) having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

forming a second isolation trench portion (a trench portion that has an angle of A2) within and extending below the first isolation trench portion (a trench portion that has an angle of A1),

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the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

filling the first and second isolation trench portions with dielectric material (4a) (column 5, line 34 – column 7, line 4).

Regarding claim 2, Sakai et al. disclose the first angle of the first trench is about 45 – 80 degrees (column 6, lines 19-21). In addition, the first angle of the first trench can also be less than 83 degrees and the first angle of the first trench is less than the second angle of the second trench (column 5, lines 56-58). Therefore, Sakai et al. teach forming a second isolation trench portion includes forming the second angle to be between eighty and ninety degrees (see figures 1, 2a-f).

Regarding claim 3, Sakai et al. teach forming a first isolation trench portion includes forming the first angle to be in a range of from about thirty degrees to about seventy degrees (column 6, lines 19-21) and forming a second isolation trench portion includes forming the second angle to be more than eighty degrees (column 5, lines 56-58) (see figures 1, 2a-f).

Regarding claim 4, Sakai et al. teach forming the isolation trench is formed in a semiconductor [1] comprises silicon (column 5, lines 38-40; column 5, lines 61-65).

Regarding claim 12, Sakai et al. teach forming the first isolation trench portion comprises forming the first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment (see figures 1, 2a-f).

Regarding claim 1, Sakai et al. (figures 7, 8(a)-(d)) teach a method of forming an isolation trench in a semiconductor comprising:

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forming a first isolation trench portion (a trench portion that has an angle of A1) having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

forming a second isolation trench portion (a trench portion that has an angle of A2) within and extending below the first isolation trench portion (a trench portion that has an angle of A1), the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

filling the first and second isolation trench portions with dielectric material (4) (column 9, line 25 – column 10, line 13).

Regarding claim 10, Sakai et al. teach forming the first isolation trench portion (a trench portion that has an angle of A1) comprises forming the first isolation trench portion having a first depth about 3.75 to 37.5 percent of a total trench depth (see figures 8a-d; column 9, lines 42-63). Sakai et al. show the first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 8, 13, 19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. as applied to claim 1 above, and further in view of US Patent No. 6,258,688 to Tsai.

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Regarding claim 8, Sakai et al. (figures 1, 2a-f, 3) differ from the claimed invention by not forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including  $\text{CF}_4$  and  $\text{CHF}_3$ . However, Tsai teaches forming the isolation trench portion comprises plasma etching using compound gases of  $\text{CF}_4$  and  $\text{CHF}_3$  (column 5, lines 18-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tsai into the method taught by Sakai et al. because it reduces the size of the trench.

Neither Sakai et al. nor Tsai teach forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  $\text{CF}_4/\text{CHF}_3 = 0.11$  to  $0.67$ . It would have been obvious to one having ordinary skill in the art at the time the invention was made to find the optimal ratio of the gases of  $\text{CF}_4$  and  $\text{CHF}_3$ , since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 13, Sakai et al. teach a method of forming an isolation trench in a surface of a silicon wafer comprising: forming a mask on the surface, the mask including an opening and sidewalls (see figures 1, 2a-f, 3; column 5, line 61 – column 6, line 58). Sakai et al. differ from the claimed invention by not etching the silicon surface using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  to form a first isolation trench portion. However, Tsai teaches forming the isolation trench portion comprises plasma etching using compound gases of  $\text{CF}_4$  and  $\text{CHF}_3$  (column 5, lines 18-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tsai into the method taught by Sakai et al. because it reduces the size of the trench.

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Neither Sakai et al. nor Tsai teach forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  $\text{CF}_4/\text{CHF}_3 = 0.11$  to  $0.67$ . It would have been obvious to one having ordinary skill in the art at the time the invention was made to find the optimal ratio of the gases of  $\text{CF}_4$  and  $\text{CHF}_3$ , since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 19, Sakai et al. teach forming a silicon nitride layer (6) on the semiconductor surface (1); and forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls (see figures 2a-f; column 5, line 61 – column 6, line 2).

Regarding claim 21, Sakai et al. teach forming a second isolation trench portion (a trench portion that has an angle of  $A_2$ ) within and extending below the first isolation trench portion (a trench portion that has an angle of  $A_1$ ), the second isolation trench portion (a trench portion that has an angle of  $A_2$ ) having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle (see figures 1, 2a-f) (column 5, line 34 – column 6, line 58).

7. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,258,688 to Tsai.

Regarding claim 13, Tsai teaches (figures 1-3) a method of forming an isolation trench (22) in a surface of a silicon wafer (10) comprising forming a mask (18) on the surface, the mask

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including an opening and sidewalls; and forming the isolation trench portion comprises plasma etching using compound gases of  $\text{CF}_4$  and  $\text{CHF}_3$  (column 5, lines 18-38).

Neither Sakai et al. nor Tsai teach forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  $\text{CF}_4/\text{CHF}_3 = 0.11$  to  $0.67$ . It would have been obvious to one having ordinary skill in the art at the time the invention was made to find the optimal ratio of the gases of  $\text{CF}_4$  and  $\text{CHF}_3$ , since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 15, Tsai teaches forming the first isolation trench portion (22) comprises forming the first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment (see figure 3).

8. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. as applied to claim 1 above, and further in view of US Patent No. 6,258,688 to Tsai.

Regarding claim 13, Sakai et al. teach a method of forming an isolation trench in a surface of a silicon wafer comprising: forming a mask (6) on the surface, the mask (6) including an opening and sidewalls (see figures 8a-d; column 9, lines 41-65). Sakai et al. differ from the claimed invention by not etching the silicon surface using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  to form a first isolation trench portion. However, Tsai teaches forming the isolation trench portion comprises plasma etching using compound gases of  $\text{CF}_4$  and  $\text{CHF}_3$  (column 5, lines 18-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the

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invention was made to incorporate the teaching of Tsai into the method taught by Sakai et al. because it reduces the size of the trench.

Neither Sakai et al. nor Tsai teach forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  $\text{CF}_4/\text{CHF}_3 = 0.11$  to  $0.67$ . It would have been obvious to one having ordinary skill in the art at the time the invention was made to find the optimal ratio of the gases of  $\text{CF}_4$  and  $\text{CHF}_3$ , since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, Sakai et al. teach etching the silicon surface includes forming the first isolation trench portion (a trench portion that has an angle of  $A_1$ ) having a first sidewall that intersects the silicon surface at an angle in a range of from about thirty degrees to about seventy degrees (column 9, lines 44-46).

Regarding claim 15, Sakai et al. teach forming the first isolation trench portion (a trench portion that has an angle of  $A_1$ ) comprises forming the first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment (see figures 8a-d).

Regarding claim 16, Sakai et al. teach forming a second isolation trench portion (a trench portion that has an angle of  $A_2$ ) within and extending below the first isolation trench portion (a trench portion that has an angle of  $A_1$ ), the second isolation trench portion (a trench portion that has an angle of  $A_2$ ) including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle (figures 7, 8a-d).

Regarding claim 17, Sakai et al. teaching forming the first isolation trench portion (a trench portion has an angle of  $A_1$ ) comprises forming the first isolation trench portion having a

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first depth about 3.75 to 37.5 percent of a total trench depth (see figures 8a-d; column 9, lines 34-63). Sakai et al. show the first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

9. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. as applied to claim 1 above, and further in view of US Patent No. 5,874,317 to Stolmeijer.

Regarding claim 11, Sakai et al. differ from the claimed invention by not planarizing the dielectric material filling the first and second isolation trench portions. However, Stolmeijer teaches planarizing the surface of the insulating layer (see figure 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Stolmeijer into the method taught by Sakai et al., since it reduces the size of the device.

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. and Tsai as applied to claim 13 above, and further in view of US Patent No. 5,874,317 to Stolmeijer.

Regarding claim 18, Sakai et al. teach filling the first and second isolation trench portions with dielectric material (4) (see figures 7, 8a-d). Sakai et al. differ from the claimed invention by not planarizing the dielectric material filling the first and second isolation trench portions. However, Stolmeijer teaches planarizing the surface of the insulating layer (see figure 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Stolmeijer into the method taught by Sakai et al., since it reduces the size of the device.

11. Claims 22, 24, 27-29 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,969,393 to Noguchi. in view of US Patent No. 6,274,457 to Sakai et al.

Regarding claim 22, Noguchi (figures 2A-4B) teaches a method of forming an isolation trench isolated transistor comprising:

forming first and second trenches disposed to a respective side of a portion of silicon,  
forming the first and second isolation trenches;

filling the first and second isolation trench portions with dielectric material (103);

forming a gate (108) extending across the silicon portion from the first isolation trench to the second isolation trench; and

forming source and drain regions (109) extending between the first and second isolation trench portions, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

Noguchi differs from the claimed invention by not forming a mask on the surface, the mask including first and second openings corresponding to the first and second isolation trenches; forming a first isolation trench portion in each of the first and second openings, each first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and forming a second isolation trench portion within and extending below each of the first isolation trench portions, the second isolation trench portions having a second depth and including a second sidewall intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater than the first angle. However, Sakai et al. teach forming a mask (column 5, line 65 – column 6, line 5) on the surface, the mask

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including first and second openings corresponding to the first and second isolation trench portions; forming a first isolation trench portion (a trench portion that has an angle of A1) in the openings, the first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and forming a second isolation trench portion (a trench portion that has an angle of A2) within and extending below the first isolation trench portion (a trench portion that has an angle of A1), the second isolation trench portion (a trench portion that has an angle of A2) having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle (see figures 1, 2a-f, 3; column 5, line 34 – column 6, line 58). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the trench-forming method of Sakai et al. into the first and second isolation trench-forming methods of Noguchi because it provides good electrical characteristics to the device isolation region.

Regarding claim 24, the combined device teaches forming a silicon nitride layer on the semiconductor surface; and forming a mask layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls (see figures 1, 2a-f of Sakai et al.; column 5, line 61 – column 6, line 2).

Regarding claim 27, Noguchi differs from the claimed invention by not forming a first isolation trench portion comprises forming a first isolation trench portion having a first sidewall intersecting a surface of the semiconductor at an angle in a range of from about thirty degrees to about seventy degrees. However, Sakai et al. teach forming a first isolation trench portion

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comprises forming a first isolation trench portion having a first sidewall intersecting a surface of the semiconductor at an angle in a range of from about thirty degrees to about seventy degrees (column 6, lines 19-21). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sakai et al. into the method taught by Noguchi because an electric field can be restrained from concentrating on an edge portion of the device isolation region.

Regarding claim 28, the combined device teaches forming a first isolation trench portion comprises forming a first isolation trench portion including a side at least some of which forms a substantially straight linear segment (see figure 1 of Sakai et al.).

Regarding claim 29, Noguchi differs from the claimed invention by not forming a second isolation trench portion comprises forming a second isolation trench portion having a second sidewall forming an angle of more than eighty degrees with the surface. However, Sakai et al. teach forming a second isolation trench portion comprises forming a second isolation trench portion having a second sidewall forming an angle of more than eighty degrees with the surface (column 5, lines 56-58). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sakai et al. into the method taught by Noguchi because an electric field can be restrained from concentrating on an edge portion of the device isolation region.

Regarding claim 32, the combined device teaches forming a gate comprises forming a gate comprising polysilicon.

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12. Claims 22 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,969,393 to Noguchi. in view of US Patent No. 6,274,457 to Sakai et al.

Regarding claim 22, Noguchi (figures 2A-4B) teaches a method of forming an isolation trench isolated transistor comprising:

forming first and second trenches disposed to a respective side of a portion of silicon,  
forming the first and second isolation trenches;

filling the first and second isolation trench portions with dielectric material (103);

forming a gate (108) extending across the silicon portion from the first isolation trench to the second isolation trench; and

forming source and drain regions (109) extending between the first and second isolation trench portions, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

Noguchi differs from the claimed invention by not forming a mask on the surface, the mask including first and second openings corresponding to the first and second isolation trenches; forming a first isolation trench portion in each of the first and second openings, each first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and forming a second isolation trench portion within and extending below each of the first isolation trench portions, the second isolation trench portions having a second depth and including a second sidewall intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater than the first angle. However, Sakai et al. teach forming a mask (column 5, line 65 – column 6, line 5) on the surface, the mask

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including first and second openings corresponding to the first and second isolation trench portions; forming a first isolation trench portion (a trench portion that has an angle of A1) in the openings, the first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and forming a second isolation trench portion (a trench portion that has an angle of A2) within and extending below ~~each~~ of the first isolation trench portion (a trench portion that has an angle of A1), the second isolation trench portion (a trench portion that has an angle of A2) having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle (see figures 7, 8a-d; column 9, line 25 – column 10, line 15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the trench-forming method of Sakai et al. into the first and second isolation trench-forming methods of Noguchi because it provides good electrical characteristics to the device isolation region.

Regarding claim 30, Sakai et al. teaching forming the first isolation trench portion <sup>a</sup>(trench portion has <sup>an</sup> angle of A1) comprises forming the first isolation trench portion having a first depth about 3.75 to 37.5 percent of a total trench depth (see figures 8a-d; column 9, lines 34-63). Sakai et al. show the first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

13. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi and Sakai et al. as applied to claim 22 above, and further in view of US Patent No. 6,258,688 to Tsai.

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Regarding claim 23, the combined device teaches forming a first isolation trench portion (a trench portion that has an angle of A1) comprises etching the silicon surface. Noguchi and Sakai et al. differ from the claimed invention by not etching the silicon surface using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  to form a first isolation trench portion. However, Tsai teaches forming the isolation trench portion comprises plasma etching using compound gases of  $\text{CF}_4$  and  $\text{CHF}_3$  (column 5, lines 18-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tsai into the method taught by Noguchi and Sakai et al. because it reduces the size of the trench.

Noguchi, Sakai et al. and Tsai differ further from the claimed invention by not forming the first isolation trench portion comprises plasma etching the silicon surface using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  $\text{CF}_4/\text{CHF}_3 = 0.11$  to  $0.67$ . It would have been obvious to one having ordinary skill in the art at the time the invention was made to find the optimal ratio of the gases of  $\text{CF}_4$  and  $\text{CHF}_3$ , since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

14. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi and Sakai et al. as applied to claim 22 above, and further in view of US Patent No. 5,874,317 to Stolmeijer.

Regarding claim 31, Noguchi and Sakai et al. differ from the claimed invention by not planarizing the dielectric material filling the first and second isolation trench portions. However, Stolmeijer teaches planarizing the surface of the insulating layer (see figure 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was

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made to incorporate the teaching of Stolmeijer into the method taught by Sakai et al., since it reduces the size of the device.

***Allowable Subject Matter***

Claims 5-7 and 9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C 112, second paragraph, set forth in this office action and to include all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QVU  
November 4, 2002

Steven Loh